CLAIMS

What is claimed is:

1. A method comprising:

issuing a load instruction to an execution cluster in an out of order processor; and

allocating an entry for the load instruction in a structure for tracking only load instructions only if the load instruction utilizes speculative data.

2. The method of claim 1, further comprising:

indicating the load instruction that uses speculative data is to be checked at retirement; and

searching the structure for tracking only load instructions for the entry for the load instruction to confirm the load data at the time of retirement.

3. The method of claim 1, further comprising:

invalidating the entry for the load instruction during a store instruction retirement if the store instruction conflicts with the load instruction.

4. The method of claim 2, further comprising:

flushing a pipeline if the structure for tracking only load instructions does not contain a valid entry for the load instruction at load instruction retirement.

5. The method of claim 1, wherein the load instruction is an advanced load instruction.

6. The method of claim 5, further comprising:

converting a basic load instruction into an advanced load instruction.

7. The method of claim 1, wherein the structure for tracking load instructions is an advanced load allocation table.

8. A device comprising:

a store queue in an out of order processor to track only store instructions; and

a load queue coupled to the store queue to track only speculative load instructions.

9. The device of claim 8, further comprising:

an instruction scheduler coupled to the store queue to schedule instruction execution; and

a reorder buffer coupled to the instruction scheduler to track program order of instructions and to track speculative load instructions to be checked at retirement.

10. The device of claim 8, wherein the load queue is an advanced load allocation table.

11. A system comprising:

a first processor having at least a 64 bit architecture comprising a first data cache, set of execution units, out of order instruction scheduler coupled to the data cache and set of execution units, a store queue coupled to the instruction scheduler to store track only store instructions and a load queue coupled to the store queue to track only speculative load instructions;

a bus coupled to the processor; and

a system memory device coupled to the bus.

12. The system of claim 11 further comprising:

a second processor coupled to the bus comprising a second data cache.

13. The system of claim 11, wherein the processor further comprises:

a reorder buffer to track program order of instructions and to track speculative load instructions to be checked at retirement.

14. An apparatus comprising:

means for tracking only speculative load instructions; and

means for tracking all instructions in program order coupled to the means for tracking only speculative instructions, comprising a field to indicate a load instruction is to be checked at retirement.

15. The apparatus of claim 14, further comprising:

means for tracking only store instructions coupled to means for tracking only speculative load instructions.

16. The apparatus of claim 14, further comprising:

means for flushing a pipeline upon detection that a speculative load is not present in the means for tracking only speculative loads at the time of load instruction retirement.

17. A machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

tracking only a set of load instructions relying on speculative data in a first data structure of an out of order processor; and

tracking a set of instructions in program order in a second data structure having a field to indicate to check speculation in a load instruction at a time of load instruction retirement.

18. The machine readable medium of claim 17, having instructions stored therein which when executed causes a machine to perform a set of operations further comprising:

tracking only a set of store instructions in a store queue of the out of order processor.

19. The machine readable medium of claim 17, having instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

invalidating allocated load instruction entries during store instruction retirement.

20. The machine readable medium of claim 17, wherein the first data structure is an advanced load allocation table.

21. The machine readable medium of claim 17, wherein the second data structure is a reorder buffer.